Claims

Sub B3

1 A content addressable memory comprising a CAM control logic unit (11) and a plurality of cells (10) connected in a chain, each cell comprising:

a memory block (12) coupled to a common address bus (ADD);

a comparator (14) coupled to a common data bus (DATA) and to the data interface of the memory block (12);

switching means (15) coupling the data interface of the memory block with the data bus, and;

a logic block (13) including a Match flip-flop (16):

the memory being operable:

in a Search phase to serially match a sequence of words on the common data bus (DATA) with the contents of a sequence of addresses in the memory blocks (12) of the cells (10); and

in an Access phase, to render the cells matched in the Search phase serially available for access via the common address and data buses (ADD and DATA).

2 A content addressable memory according to claim 1 wherein each cell contains a memory block (12), a logic block (13), a comparator (14), and a bidirectional switch (15).

A 3 A content addressable memory according to ~~either previous claim~~ claim 1 implemented on an integrated circuit chip.

4 A content addressable memory according to claim 3 wherein several such chips can be chained.

5 A content addressable memory according to claim 4 wherein each chip includes a control unit which can be disabled.

A 6 A content addressable memory according to ~~any previous claim~~ claim 1 including a MASK bus input which determines which bits of the words of the sequence of words are used for matching in the Search phase.

7 A content addressable memory according to ~~any previous claim~~ claim 1 including a return line from the end of the chain of cells back to the CAM control unit 11 which changes state when all Match flip-flops in the chain have been accessed.

8 A method of operating a content addressable memory according to ~~any previous claim~~ claim 1 wherein a standard byte address is chosen in all data blocks and a byte different from the inactive state of the data bus is included in that address in every data block.

9 A method of operating a content addressable memory according to ~~any previous claim~~ claim 1 wherein each cell is divided into a plurality of distinct data blocks.

10 A method of operating a content addressable memory according to ~~any previous claim~~ claim 1 wherein a plurality of cells are combined into an extended data block with all cells of the block containing corresponding key fields.

11 A method of operating a content addressable memory according to ~~any previous claim~~ claim 1 wherein a standard byte address is chosen in all data blocks and filled with one data value if the data block in that cell is valid and another data value if the data block in the cell is cleared, ie invalid.

12 ~~Any novel and inventive feature or~~ combination of features specifically disclosed herein within the meaning of ~~Article 4H of the International~~ Convention (Paris Convention).